## REMARKS

### *Claim Disposition*

Claims 1 – 12 are pending in the present application. Claims 2 – 4 have been allowed. Claims 1 and 5 – 12 have been rejected. Claim 9 has been amended to more particularly point out and distinctly claim that which Applicant claims as his invention. Applicant appreciates the Examiner's indication of the allowance of claims 2 – 4.

### *Objections*

The drawings have been objected to under 37 CFR 1.83(a). The Examiner states:

> "The drawings must show every feature of the invention specified in the claims. Therefore the recited different setting of the transistors contained in the pull-up and pull-down circuits respectively in Claim 7 must be shown or the feature(s) canceled from the claim(s)."

Applicant appreciates the Examiner's suggestion that the drawings must show every feature of the invention specified in the claims. However, Applicant respectfully contends that the requested "settings" of the transistors are an operational state of the device depicted in the figures and would not need to be depicted. However, should the Examiner not find this argument persuasive, a figure corresponding to the teachings of the specification could be provided to address the Examiner's concerns.

### *Claim Rejections Under 35 U.S.C. § 103*

Claims 1 and 5 - 12 stand rejected under 35 U.S.C. § 103 (a) as being unpatentable over Rosefield *et al.*, U.S. Patent No. 6,541,996, hereinafter referred to as Rosefield; in view of Levin *et al.*, U.S. Patent No. 6,751,782, hereinafter referred to as Levin. Applicant respectfully traverses. With respect to Claims 1, 5-6, and 8 and 10, Rosefield is cited in the Office Action as allegedly disclosing:

> "a method (see Figs 1-4) for measuring the impedance of driver devices (102, IMPEDANCE MEASUREMENT) during a test (see Fig. 2, pull up test EN and pull down test EN) being carried out before the regular

operation of the semiconductor device (chip), the driver device (102 of the semiconductor device including each a pull-up circuit (204, pull up impedance matching array) and a pull-down circuit (206, pull down impedance matching array) (Col. 2, lines 54 – 65 'on-chip programmable pull up impedance matching array", the method comprising:"

"activating of both the pull-up circuit (see Fig. 3, step 301 enable pull up imped array) and the pull-down circuit (see Fig 3, step 308 enable pull down imped array),"

"determining a voltage dropping over the pull-up and/or pull-down circuit (see Col. 3, lines 59-60 "voltage drop"),"

"determining a total impedance of he pull up and pull down circuits (see Col. 9, lines 21-22 and 27-29)."

It is acknowledged in the Final Office Action that Rosefield "do[es] not disclose that their both pull-up and pull-down circuits are activated substantially simultaneously and do[es] not disclose the step of determining a first current flowing through the pull-up circuit or the pull-down circuit respectively."

Levin is cited in the Final Office Action for allegedly disclosing:

"a method and apparatus for analog compensation of driver output signal slew rate against device impedance variation (see Figs. 5-6) comprising a pull up circuit (410, pull-up devices) and pull down circuit (420, pull-down devices). Levin et al ('782) exclusively teaches the step of simultaneously activation both the pull-up circuit (410) and pull-down circuit (420) (see Col. 6, lines 55-56 "pull-down devices 420 will generally be turned off and simultaneously, one or more of the pull-up devices 410 may be turned on"). Furthermore Levin et al ('782 disclose the step of determining a first current (490,494) flowing through a pull-up circuit (410) or pull-down circuit (420) respectively".

It is suggested in the Office Action that it would have been obvious to incorporate the step of simultaneously activating both the pull-up and pull-down circuits as taught by Levin et al ('782) into Rosefield et al ('996)'s method for the purpose of providing analog compensation of a driver output signal slew rate against device impedance variation as disclosed by Levin et al. ('782) (see Abstract)

The Examiner further states:

> "With respect to claim 11, Rosefield et al (6996) discloses that a test device (comparator 209) is a test device not used for the driving of output signals during the regular operation of the semiconductor device and is for selecting the driver setting for at least one other semiconductor device (chip) during the test carried out before the regular operation of the at least one other semiconductor device (chip)."
>
> "With respect to claim 12, Rosefield et al ('996) discloses that the test device (comparator 209) is connected with a device (208) provided on the semiconductor device (chip) itself, by means of which a voltage dropping over the pull-up and/or pull-down circuit is determined."

For an obviousness rejection to be proper, the Examiner must meet the burden of establishing a *prima facie* case of obviousness. *In re Fine*, U.S.P.Q.2d 1596, 1598 (Fed. Cir.1988). The Examiner must meet the burden of establishing that all elements of the invention are disclosed in the prior art; that the prior art relied upon, coupled with knowledge generally available in the art at the time of the invention, must contain some suggestion or incentive that would have motivated the skilled artisan to modify a reference or combined references; and that the proposed modification of the prior art must have had a reasonable expectation of success, determined from the vantage point of the skilled artisan at the time the invention was made. *In re Fine*, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988); *In re Wilson*, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970); *Amgen v. Chugai Pharmaceuticals Co.*, 927 U.S.P.Q.2d, 1016, 1023 (Fed. Cir.1996).

Further, even assuming that all elements of an invention are disclosed in the prior art, an Examiner cannot establish obviousness by locating references that describe various aspects of a patent applicant's invention without also providing evidence of the motivating force which would have impelled one skilled in the art to do what the patent applicant has done. *Ex parte Levengood*, 28 U.S.P.Q. 1300 (Bd. Pat. App. Int. 1993). Finally, for an obviousness rejection to be proper, the Examiner must meet the burden of establishing ... that the proposed modification of the prior art must have had a reasonable expectation of success. MPEP 2143.02. Moreover, the suggested modification cannot change the principle of operation of a reference. MPEP 2143.01.

Applicant respectfully contends that neither Rosefield nor Levin, whether alone, or in combination, teaches or discloses each element of the claimed invention. Applicant respectfully disagrees with the Examiner's interpretation that the combination of Rosefield and Levin suggests a method for measuring and trimming the impedance of a driver device in a semiconductor device during a test being carried out before the regular operation of the semiconductor device, with substantially simultaneously activating of both the pull-up circuit and pull-down circuit; and determining a first current flowing through the pull-up circuit or the pull-down circuit, respectively, with substantially simultaneously activated pull-up and pull-down circuits during the test carried out before the regular operation of the semiconductor device.

In particular, Levin does not teach or disclose the step of **determining a first current flowing through the pull-up or the pull-down circuit, respectively with substantially simultaneously activated pull-up and pull-down circuits**. To support the rejection, the Examiner has relied upon Levin at Figure 5, reference numerals 490, 494 as allegedly disclosing the claimed element. However, Levin does not teach or disclose **determining a first current** ... **with substantially simultaneously activated** pull-up and pull down circuits as the Examiner suggests. In other words, while Levin does teach, "generating a crowbar current" and then sweeping the resistances, (See Figs. 5, 6, 7A, B, C and 10 as well as Col. 7 line 25 – Col. 8 line 11), it does not teach or disclose actually "*measuring the current*" with substantially simultaneously activated pull-up and pull-down circuits. It is important to appreciate and recognize that there is a functional distinction between the process step of actually "*measuring the current*" as compared with Levin's **establishing** or generating a current and then reacting to it (that is, without actually measuring it). This distinction provides a significant advantage to the claimed invention over the existing art. In particular, for example, the value of the driver device impedance can be determined and trimmed more accurately than in the prior art. To reiterate for clarity, in the claimed invention, as the current is measured, the real value of the current is taken into account and the appropriate compensation for the device impedance computed. Conversely, with the system of Levin, the effects of the crowbar current are compensated merely to achieve a slew rate within a preselected tolerance.

A further, and significant advantage to measuring the actual current with substantially simultaneously activated pull-up and pull-down circuits is that the measurement may also be further corrected by subtracting an additional measured current from the current measured with substantially simultaneously activated pull-up and pull-down circuits. The standby current, for example, might be measured with deactivated pull-up and pull-down circuits. Thereby, even further enhanced impedance trimming accuracy might be achieved. This distinction is further exemplified by the Examiner's allowance of Claim 2, which includes limitations directed to such functionality.

In contrast, Levin merely teaches establishing a crowbar current. Then Levin automatically adjusts the compensation resistance value to get the desired slew rate of the drivers within a range that is acceptable, without "measuring the current with substantially simultaneously activated pull-up and pull-down circuits".

In conclusion, neither Rosefield nor Levin, teaches or discloses numerous elements of the claims. Therefore, neither Rosefield nor Levin, whether alone or in combination cannot render Applicant's claims unpatentable. Thus, Claim 1 is patentable; the rejection is improper and should be withdrawn.

In view of the above discussion, Claims 5 - 12 depend from Claim 1, and include all of the corresponding limitations thereof. Claim 1 is not taught by Rosefield or Levin, whether alone or in combination, therefore, Claims 5 - 12 cannot be taught by Rosefield or Levin either. Thus, Claims 5 – 12 are allowable; the rejections are improper and they should be withdrawn.

Therefore, the Examiner has not made a *prima facie* case for obviousness, and Claims 1 and 5 -12 may not be rendered unpatentable as suggested. Therefore, Claims 1 and 5 - 12 are allowable, the rejections are improper, and they should be withdrawn.

Claim 7 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Rosefield et al., U.S. Patent No. 6,541,996, hereinafter referred to as Rosefield; in view of Levin et al., U.S. Patent No. 6,751,782, *hereinafter referred to as Levin, as applied to Claim 1 above, in further view of Kwon et* al., U.S. Patent No. 6,115,298, hereinafter

referred to as Kwon. Applicant respectfully traverses. With respect to Claim 7, it is acknowledged in the Office Action that "Rosefield *et al* ('996) in view of Levin *et al* ('782) do not disclose that one or several of the method steps are performed several times in sequence, each with different settings of transistors contained in the pull-up or pull-down circuits, respective. Kwon *et al.* is cited as allegedly disclosing:

> "a semiconductor device with automatic impedance adjustment circuit (see Figs. 3-4) comprising a first transistor array 107 and a second transistor array 108. Kwon *et al* ('298) exclusively teach that one or several of the method steps are performed several times in sequence, each with different settings of transistors contained in the pull-up or pull down circuits (see Col. 6, lines 6-13)."

It is further suggested in the Office Action that it would have been obvious to incorporate the teaching of Kwon *et al* ('298) into Rosefield *et al* ('996)' in view of Levin *et al* ('782)'s method for the purpose of providing an impedance adjustment circuit for matching the impedance of the data driver circuit with signal line impedance of the bus as disclosed by Kwon *et al* ('298). (See, *e.g.*, Col. 1, lines 61-64.)

Applicant respectfully contends that neither Rosefield, Levin, nor Kwon whether alone, or in combination, teaches or discloses each element of the claimed invention. As presented for Claim 1 above, Applicant respectfully disagrees with the Examiner's suggested interpretation that the combination of Rosefield, Levin, and Kwon suggests a method for measuring and trimming the impedance of a driver device in a semiconductor device during a test being carried out before the regular operation of the semiconductor device, with substantially simultaneously activating of both the pull-up circuit and pull-down circuit; and determining a first current flowing through the pull-up circuit or the pull-down circuit, respectively, with substantially simultaneously activated pull-up and pull-down circuits during the test carried out before the regular operation of the semiconductor device; wherein the devise is a test device not used for the driving of output signals during the regular operation of the semiconductor device.

The amendments and arguments presented herein are made for the purposes of better defining the invention, rather than to overcome the rejections for patentability. The claims have not been amended to overcome the prior art and therefore, no presumption should attach that either the claims have been narrowed over those earlier presented, or that subject matter or equivalents thereof to which the Applicant is entitled has been surrendered.

## CONCLUSION

It is believed that the foregoing remarks are fully responsive to the Office Action and that the claims herein should be allowable to the Applicant. Accordingly, reconsideration and allowance of Claims 1 and 5 – 12 are respectfully requested. In the event the Examiner has any queries regarding the instantly submitted response, the undersigned respectfully requests the courtesy of a telephone conference to discuss any matters in need of attention.

Respectfully submitted,

ARENDT & ASSOCIATES INTELLECTUAL PROPERTY GROUP

By Jacqueline M. Arendt
Jacqueline M. Arendt
Registration No 43,474
Attorney for Applicants

Dated: May 6, 2006

**Customer No. 44590**
ARENDT & ASSOCIATES INTELLECTUAL PROPERTY GROUP
1740 Massachusetts Avenue
Boxborough, MA 01719-2209 USA
Telephone: (978) 897-8400
Facsimile: (978) 582-5547